PC/104-PLUS 4 / 8 PORT FAST ETHERNET SWITCH MODULE

The SPIDERLAN-family consists of universal high performance, compact and robust ethernet modules for the industrial use. SPIDERLAN unifies two complete 10/100BaseTX Fast Ethernet Adapters on a single PC/104-plus board. Each network controller is combined with a integrated 5 port layer-2 switch subsystem. So the board comes with up to eight (2x4) fully independent operating external 10/100BASE-TX ports, all available on RJ45 connectors. Switched networking minimizes network loading, eliminates collisions and enables true deterministic communications. SPIDERLAN is available as compact single PC/104-*Plus* module with connectors onboard, or with separated switch sub-modules for front panel assemblies. All these features make SPIDERLAN to the ideal solution for industrial network applications, like routers, firewalls, etc.

Features

- Up to 2 AMD PCNet^{TM} Fast –III Fast Ethernet controllers on a single board
- High performance bus mastering for low CPU and bus utilisation.
- PCI specification 2.2 compliant
- 5 volt only power supply
- up to 2 integrated 5-port layer-2 ethernet switch subsystems
- up to 8 (2x4) external 10/100BaseTX ports
- onboard RJ45 connectors, or separated external switch sub-modules
- IEEE: 802.3u autonegotiation 10/100 Mbps, half/full duplex operation
- Full duplex IEEE: 802.3x support
- MDI / MDI-X autocrossover functionality
- 2 LED indicators for all ports

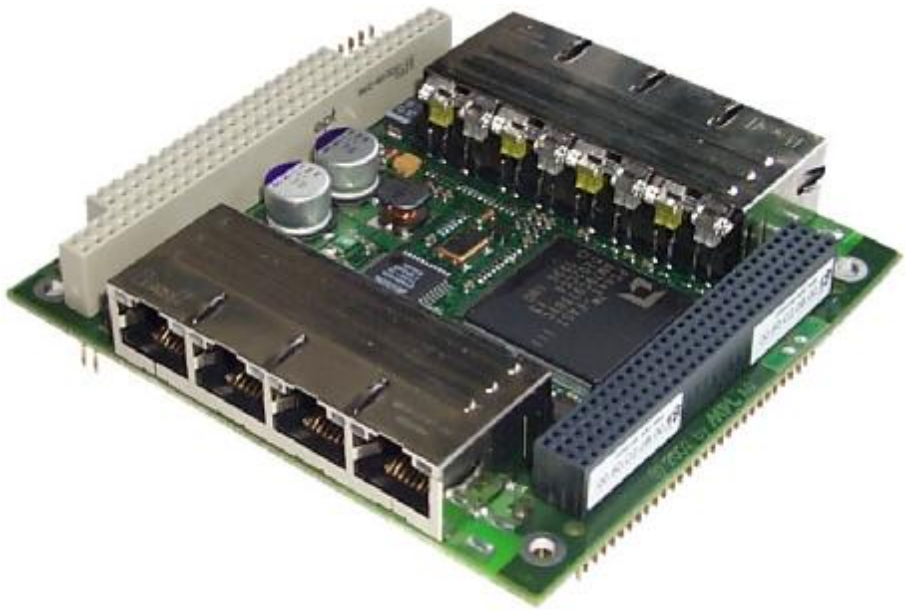


TABLE OF CONTENTS

1. INTRODUCTION

1.1 ABOUT THIS MANUAL

This manual assists the installation and initialisation procedure by providing all the information necessary to handle and configure the SPIDERLAN.
The manual is written for technical personnel responsible for integrating the SPIDERLAN into their system.

1.2 SAFETY PRECAUTIONS AND HANDLING

For personal safety and safe operation of the SPIDERLAN, follow all safety procedures described here and in other sections of the manual.

- Power must be removed from the system before installing (or removing) the SPIDERLAN to prevent the possibility of personal injury (electrical shock) and/or damage to the product.
- Handle the product carefully, i.e., dropping or mishandling the SPIDERLAN can cause damage to assemblies and components.
- Do not expose the equipment to moisture.

WARNING

There are no user-serviceable components on the SPIDERLAN

1.3 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

Various electrical components within the product are sensitive to static and electrostatic discharge (ESD). Even a non-sensible static discharge can be sufficient to destroy or degrade a component's operation!

With an open housing, do not touch any electronic components. Handle or touch only the unit chassis.

1.4 EQUIPMENT SAFETY

Great care is taken by MPL that all its products are thoroughly and rigorously tested before leaving the factory to ensure that they are fully operational and conform to specification. However, no matter how reliable a product, there is always the remote possibility that a defect may occur. The occurrence of a defect on this device may, under certain conditions, cause a defect to occur in adjoining and/or connected equipment. It is the user's responsibility to ensure that adequate protection for such equipment is incorporated when installing this device. MPL accepts no responsibility whatsoever for such kind of defects, however caused.

2. GENERAL INFORMATION AND SPECIFICATIONS

This chapter provides a general overview over the SPIDERLAN and its features. It outlines the electrical and physical specifications of the product, its power requirements and a list of related publications.

2.1 SPECIFICATIONS

ELECTRICAL

Ethernet Controller:
- single/dual AMD PCNet™ FAST III ethernet controllers
- 32-bit PCI bus master
- supports 3.3V and 5V PCI signalling
- DMA buffer management unit for low CPU and bus utilisation
- Large independent RX/TX FIFO buffers
- IEEE802.3 and Blue book ethernet compatible
- Device drivers for all major operation systems available

Ethernet Switch:
- single/dual Kendin KS8995E layer-2 ethernet switch chipset
- 1 internal port, (connected to onboard ethernet controller)
- 4 external 10/100BaseTX ports
- 128 kB SRAM for frame buffering
- 1.4Gps high performance memory bandwidth
- Lookup engine supports 1k absolute MAC addresses
- Automatic address learning, aging and migration
- Broadcast storm protection

Physical:
- Hardware based 10/100, full/half, flow control and autonegotiation
- Full duplex IEEE802.3x flow control
- Half duplex back pressure flow control

Connectors:
- single/dual onboard quad-RJ45 connectors or optionally 40 pin mini headers for the connection of external switch sub-modules

Indicators:
- indicators for link status / activity and 10/100 Mbps operation (for each port)

PHYSICAL/POWER

Form factor:
Length x width x height : 95.89 mm (3.775'') x 90.17 mm (3.550'') x 13.5 mm max.
(please refer to section 2.2)

Weight:
120g / 0.265lbs (fully equipped SPIDERLAN-2P)

Input Power :
+5VDC +- 5%

Power consumption:
Typ. 2.5W (single controller, 4ports) / 5W (dual controller, 8 ports)

ENVIRONMENT

Temperature range:
0°C to +70°C (+32°F to +158°F)
optional -40°C to +75°C (-40°F to +185°F)

Relative humidity:
10% ... 90% non condensing

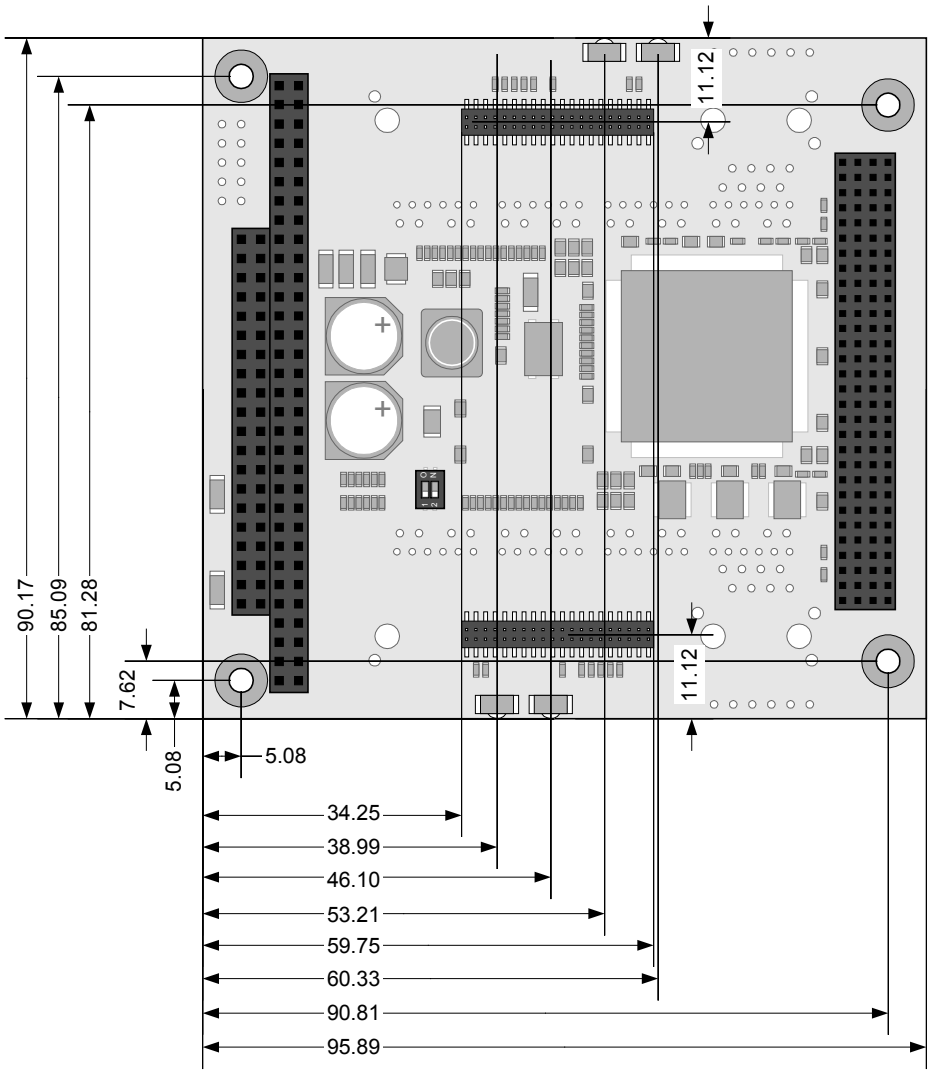
2.2 VERSION INFORMATION

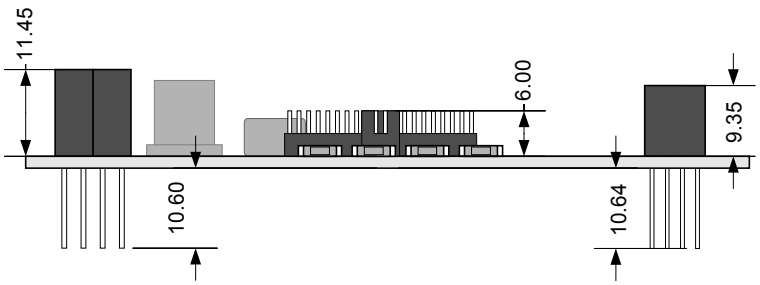
SPIDERLAN-1P:	single ethernet controller with onboard switch subsystem,
SPIDERLAN-2P:	dual ethernet controllers, each with onboard switch subsystem
SPIDERLAN-1E:	single ethernet controller with separated switch sub-module
SPIDERLAN-2E:	dual ethernet controllers with two separated switch sub-modules

2.3 DIMENSIONS

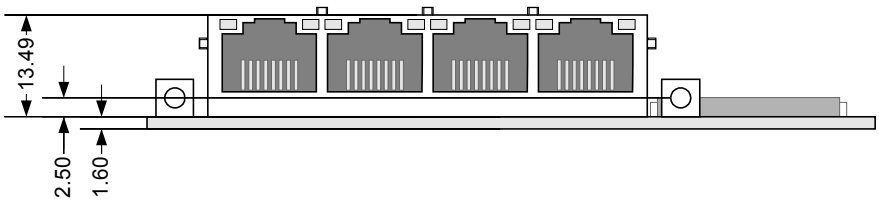
2.3.1 EXTERNAL SWITCH VERSION (SPIDERLAN-1E, SPIDERLAN-2E)

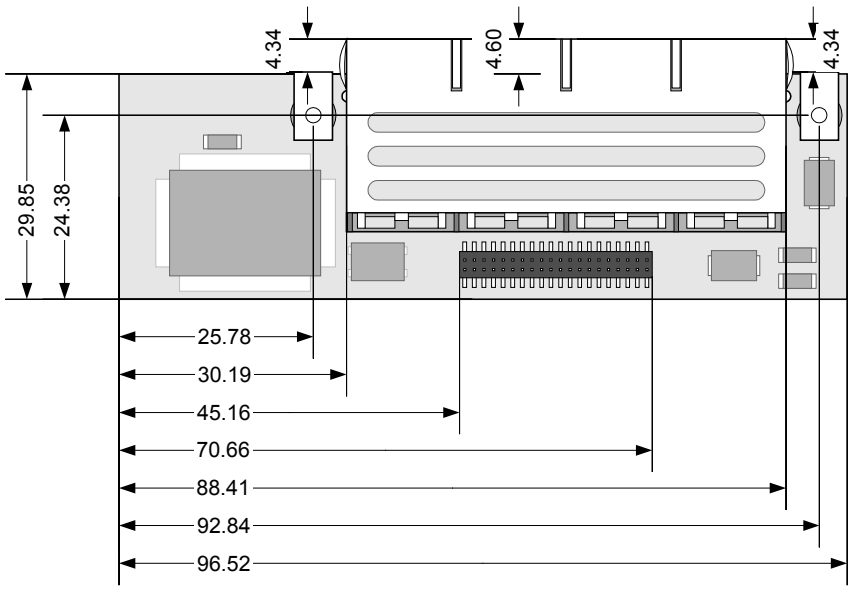
2.3.1.1 BASEBOARD



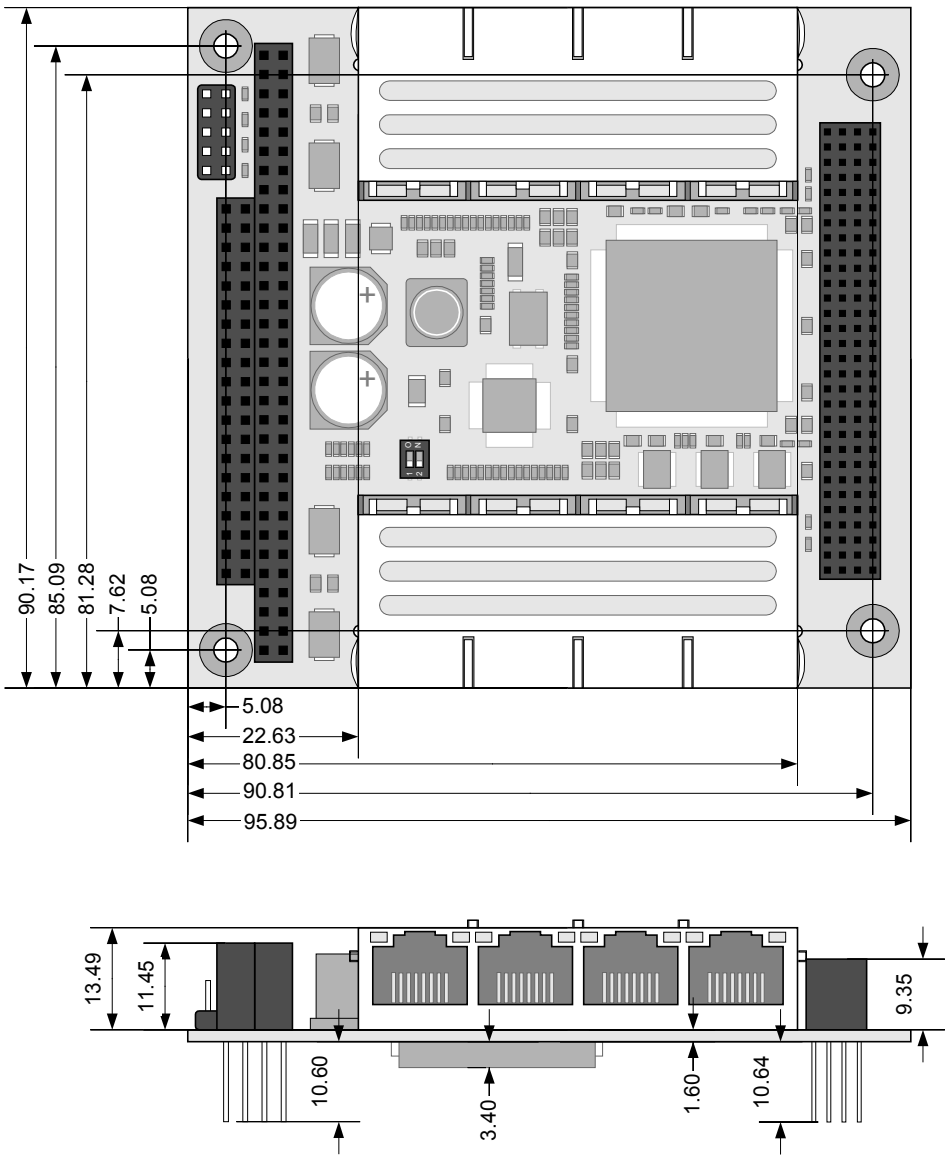


2.3.1.2 SWITCH SUBMODULE (SPIMS4)





2.3.2 ONBOARD SWITCH VERSION (SPIDERLAN-1P, SPIDERLAN-2P)

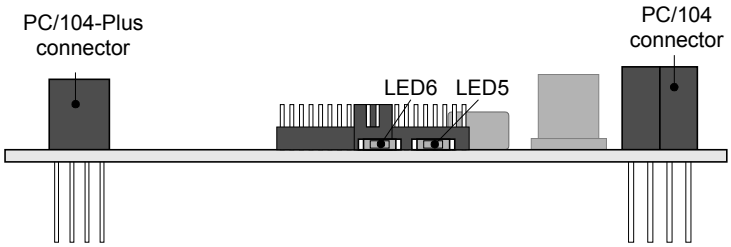


3. PREPARATION FOR USE

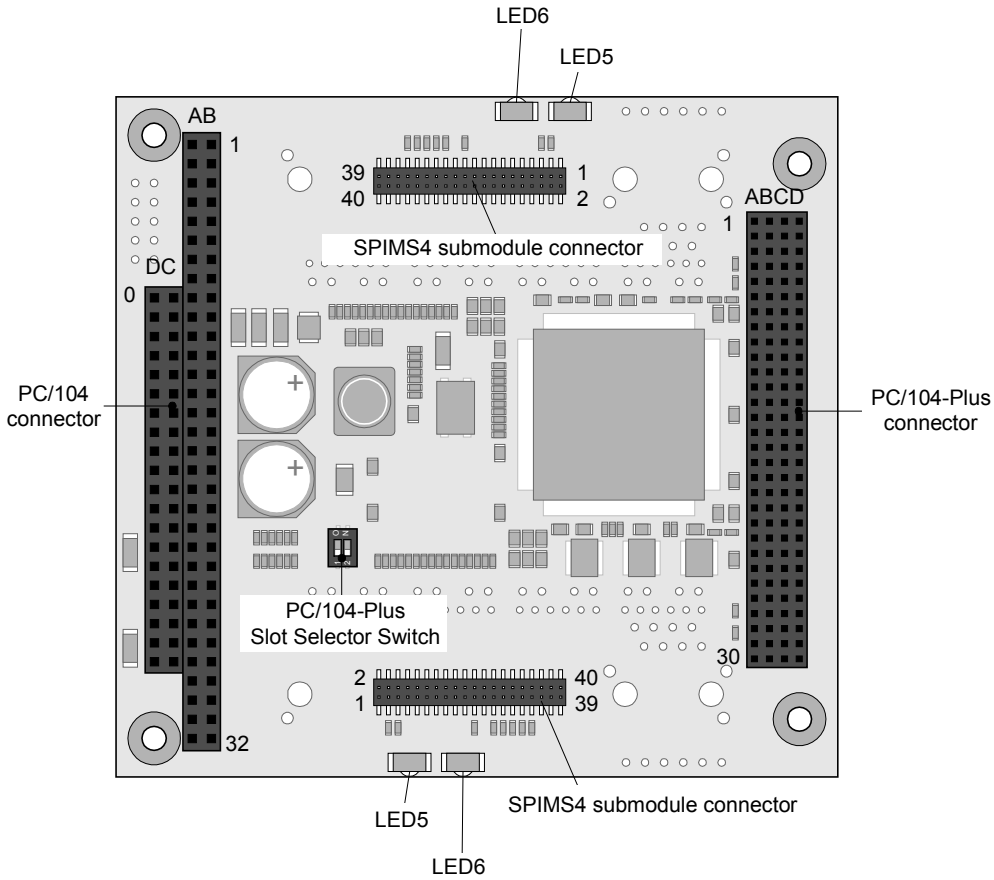
3.1 PARTS LOCATION

3.1.1 EXTERNAL SWITCH VERSION (SPIDERLAN-1E, SPIDERLAN-2E)

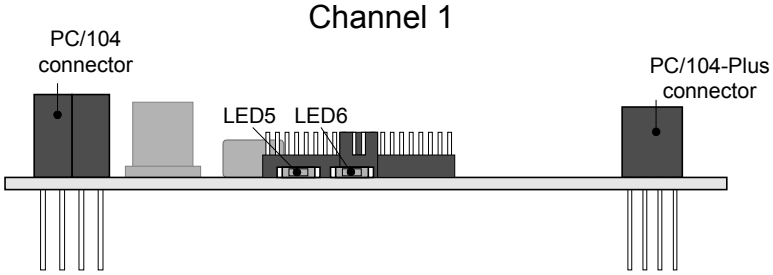
3.1.1.1 BASEBOARD



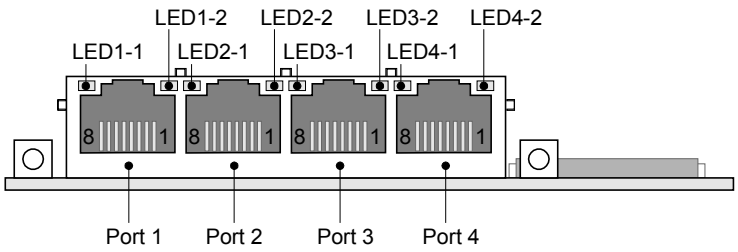
Channel 2

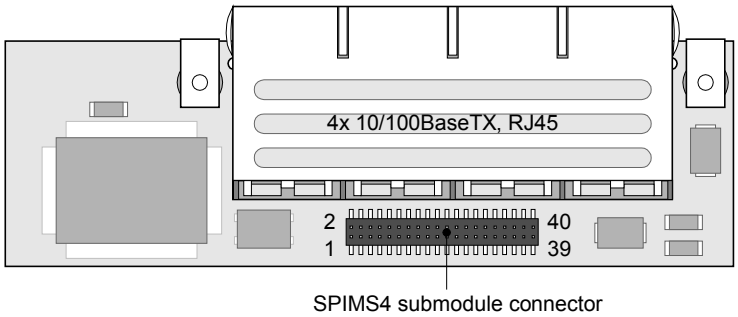


Channel 1

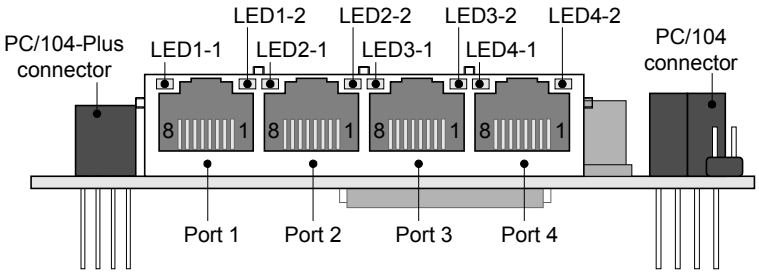


3.1.1.2 SWITCH SUBMODULE (SPIMS4)

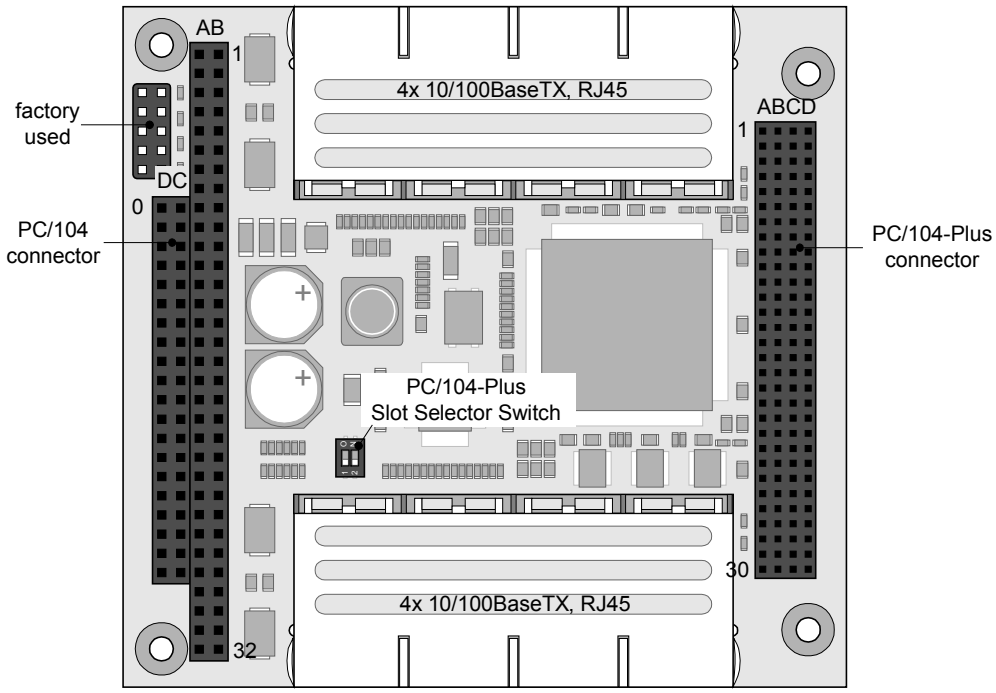




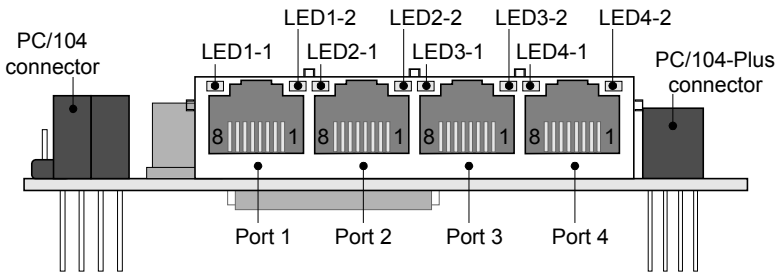
3.1.1.3 ONBOARD SWITCH VERSION (SPIDERLAN-1P, SPIDERLAN-2P)



Channel 2



Channel 1

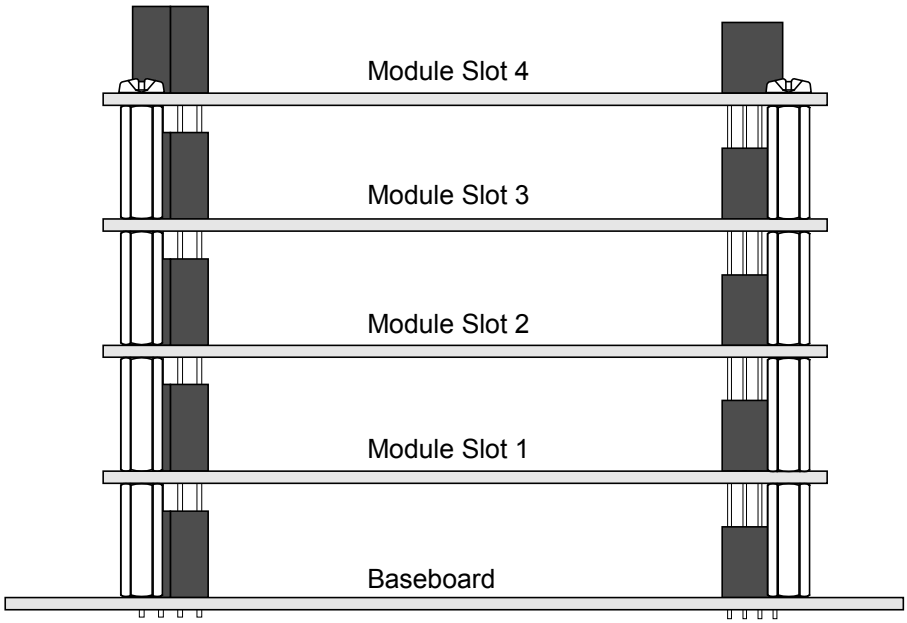


3.2 SWITCH SETTINGS

Default switch settings are in brackets.

3.2.1 PC/104-PLUS SLOT SELECTOR SWITCH

3.2.1.1 PC/104-PLUS MODULE STACK



3.2.1.2 SINGLE CHANNEL VERSION (SPIDERLAN-1P, SPIDERLAN-1E)

SW1-1	SW1-2	Ethernet Controller 1
(OFF)	(OFF)	Module Slot 1
OFF	ON	Module Slot 2
ON	OFF	Module Slot 3
ON	ON	Module Slot 4

3.2.1.3 DUAL CHANNEL VERSION (SPIDERLAN-2P, SPIDERLAN-2E)

SPIDERLAN versions, which have 2 network controllers, behave like 2 independent PC-104-plus cards. Two module slots in the PC-104-plus stack will be occupied.

SW1-1	SW1-2	Ethernet Controller 1	Ethernet Controller 2
(OFF)	(OFF)	Module Slot 1	Module Slot 2
OFF	ON	Module Slot 2	Module Slot 3
ON	OFF	Module Slot 3	Disabled
ON	ON	Module Slot 4	Disabled

3.3 CONNECTORS

3.3.1 CONNECTOR FOR SPIMS-4 MODULE (SPIDERLAN-1E, SPIDERLAN-2E)

Pin number	Signal	Description	Pinout
1	VCC	+3.3V	
2	VCC	+3.3V	
3	MDIO	Management Data Input/Output	
4	GND	Ground	
5	MDC	Management Data Clock	
6	GND	Ground	
7	RXD3	Receive Data, Bit 3	
8	GND	Ground	
9	RXD2	Receive Data, Bit 2	
10	GND	Ground	
11	RXD1	Receive Data, Bit 1	
12	GND	Ground	
13	RXD0	Receive Data, Bit 0	
14	GND	Ground	
15	RXDV	Receive Data Valid	
16	GND	Ground	
17	RXCLK	Receive Clock	
18	GND	Ground	
19	RXER	Receive Error	
20	GND	Ground	
21	TXER	Transmit Coding Error	
22	GND	Ground	
23	TXCLK	Transmit Clock	
24	GND	Ground	
25	TXEN	Transmit Enable	
26	GND	Ground	
27	TXD0	Transmit Data, Bit 0	
28	GND	Ground	
29	TXD1	Transmit Data, Bit 1	
30	GND	Ground	
31	TXD2	Transmit Data, Bit 2	
32	GND	Ground	
33	TXD3	Transmit Data, Bit 3	
34	GND	Ground	
35	COL	Collision Detected	
36	GND	Ground	
37	CRS	Carrier Sense	
38	GND	Ground	
39	VCC	+3.3V	
40	VCC	+3.3V	

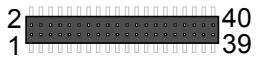


Figure 3.6

3.3.2 QUAD RJ45 – CONNECTORS

Port 1			Pinout
Pin number	Signal	Description	
1	RX1+	Receive data +	
2	RX1-	Receive data -	
3	TX1+	Transmit data +	
4	CMT	75 Ohm, common mode termination	
5			
6	TX1-	Transmit data -	
7	CMT	75 Ohm, common mode termination	
8			
Port 2			
Pin number	Signal	Description	
1	RX2+	Receive data +	
2	RX2-	Receive data -	
3	TX2+	Transmit data +	
4	CMT	75 Ohm, common mode termination	
5			
6	TX2-	Transmit data -	
7	CMT	75 Ohm, common mode termination	
8			
Port 3			
Pin number	Signal	Description	
1	RX3+	Receive data +	
2	RX3-	Receive data -	
3	TX3+	Transmit data +	
4	CMT	75 Ohm, common mode termination	
5			
6	TX3-	Transmit data -	
7	CMT	75 Ohm, common mode termination	
8			
Port 4			
Pin number	Signal	Description	
1	RX4+	Receive data +	
2	RX4-	Receive data -	
3	TX4+	Transmit data +	
4	CMT	75 Ohm, common mode termination	
5			
6	TX4-	Transmit data -	
7	CMT	75 Ohm, common mode termination	
8			

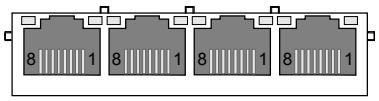
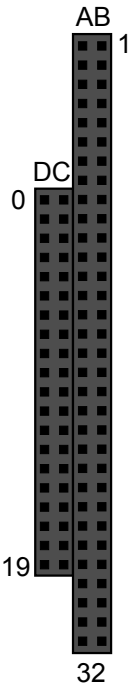


Figure 3.10

3.3.3 PC/104 INTERFACE PIN NUMBERS

Number	Row A	Row B	Row C	Row D
0	--	--	GND	GND
1	/IOCHCK	GND	/SBHE	/MEMCS16
2	SD7	RSTDRV	LA23	/IOCS16
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	/ENDXFR	LA17	/DACK0
9	SD0	+12V	/MEMR	DRQ0
10	IOCHRDY	NC	/MEMW	/DACK5
11	AEN	/SMEMW	SD8	DRQ5
12	SA19	/SMEMR	SD9	/DACK6
13	SA18	/IOW	SD10	DRQ6
14	SA17	/IOR	SD11	/DACK7
15	SA16	/DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	/DACK1	SD14	/MASTER
18	SA13	DRQ1	SD15	GND
19	SA12	/REFRESH	NC	GND
20	SA11	SYSCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	IRQ6	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4	--	--
25	SA6	IRQ3	--	--
26	SA5	/DACK2	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5V	--	--
30	SA1	OSC	--	--
31	SA0	GND	--	--
32	GND	GND	--	--



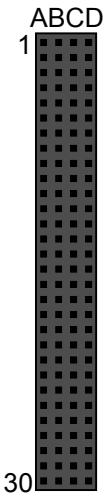
Notes:

**1* Signal not used or not available.

**2* For more detailed information refer to the PC/104 Specification, Version 2.3 and to the IEEE P996 draft standard (D2.02).

3.3.4 PC/104 PLUS INTERFACE PIN NUMBERS

Number	Row A	Row B	Row C	Row D	Pinout
1	GND	NC	+5V	AD0	
2	+5V	AD2	AD1	+5V	
3	AD5	GND	AD4	AD3	
4	C/BE0	AD7	GND	AD6	
5	GND	AD9	AD8	GND	
6	AD11	+5V	AD10	M66EN	
7	AD14	AD13	GND	AD12	
8	+3,3V	C/BE1	AD15	+3,3V	
9	SERR	GND	(SBO)*1*	PAR	
10	GND	PERR	+3,3V	SDONE	
11	STOP	+3,3V	LOCK	GND	
12	+3,3V	TRDY	GND	DEVSEL	
13	FRAME	GND	IRDY	+3,3V	
14	GND	AD16	+3,3V	C/BE2	
15	AD18	+3,3V	AD17	GND	
16	AD21	AD20	GND	AD19	
17	+3,3V	AD23	AD22	+3,3V	
18	IDSEL0	GND	IDSEL1	IDSEL2	
19	AD24	C/BE3	+5V	IDSEL3	
20	GND	AD26	AD25	GND	
21	AD29	+5V	AD28	AD27	
22	+5V	AD30	GND	AD31	
23	REQ0	GND	REQ1	+5V	
24	GND	REQ2	+5V	GNT0	
25	GNT1	+5V	GNT2	GND	
26	+5V	CLK0	GND	CLK1	
27	CLK2	+5V	CLK3	GND	
28	GND	INTD	+5V	RST	
29	+12V	INTA	INTB	INTC	
30	-12V	NC	NC	GND	

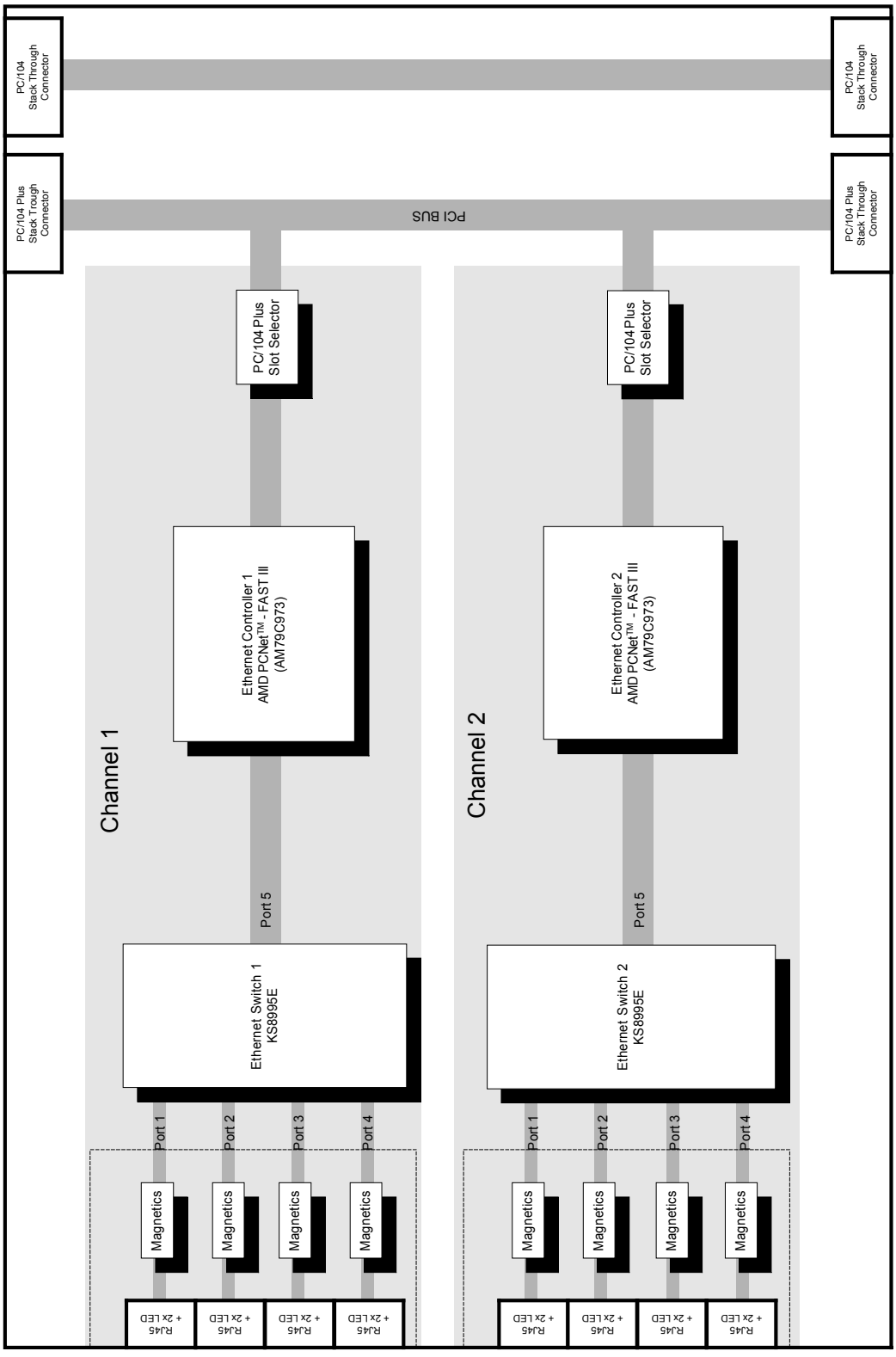


Notes:
1 Signal not available (designed for the use of max. 2 modules).
2 For more detailed information refer to the PC/104 – Plus Specification, Version 1.0 and to the PCI Specification Rev.2.1.

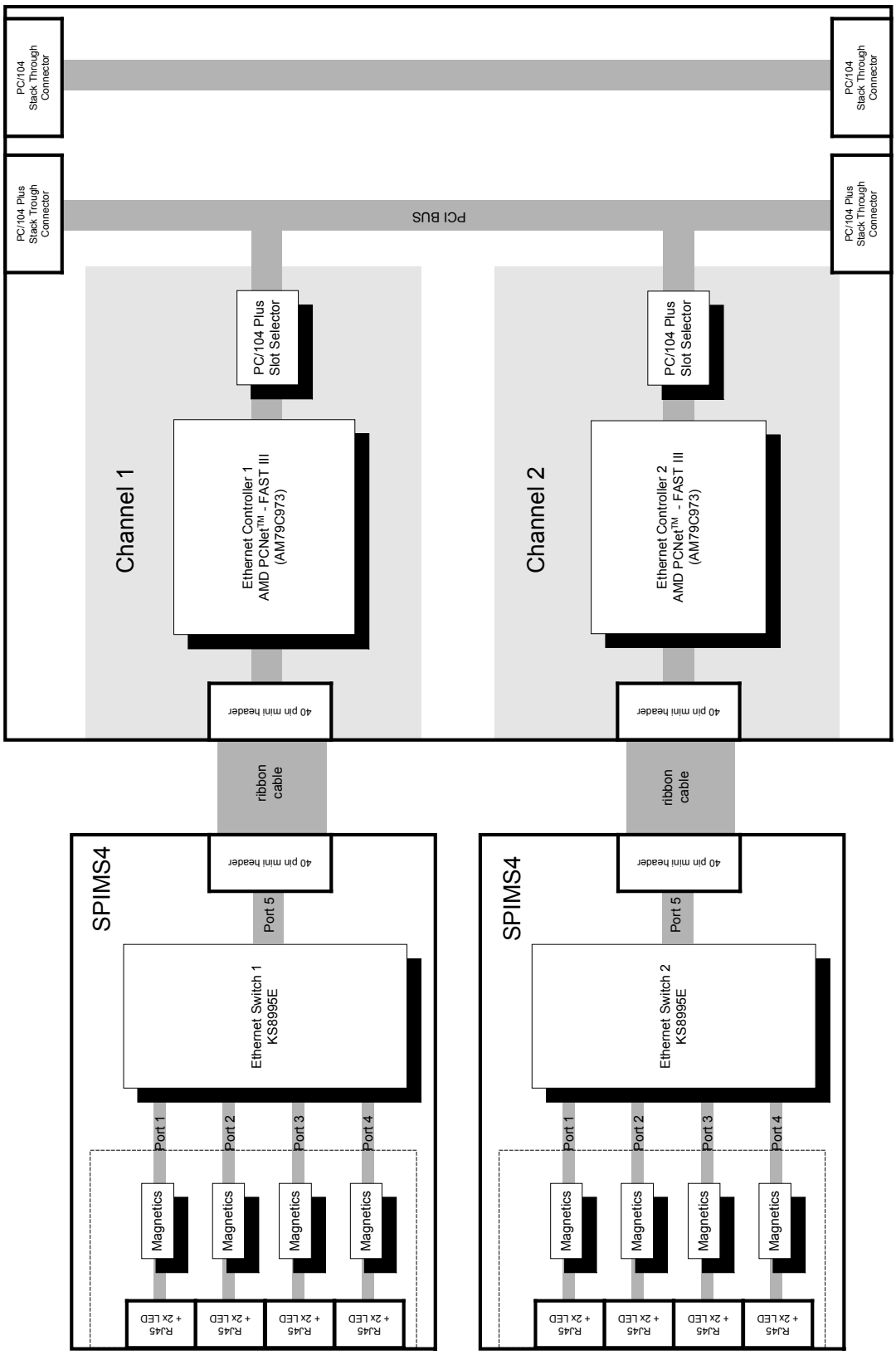
4. OPERATION

4.1 BLOCK DIAGRAM

4.1.1 ONBOARD SWITCH VERSION (SPIDERLAN-1P, SPIDERLAN-2P)



4.1.2 EXTERNAL SWITCH VERSION (SPIDERLAN-1E, SPIDERLAN-2E)



4.2 LED INDICATORS

4.2.1 INTEGRATED RJ45 CONNECTOR INDICATORS

4.2.1.1 LINK / ACTIVITY (GREEN)

On = Link Pass
Off = Link Failed, Transmit / Receive Activity

Please refer to section 3.1, port 1:LED1-1, port 2: LED2-1, port 3: LED3-1, port 4: LED4-1

4.2.1.2 10/100 MBIT (YELLOW)

On = 100MBit
Off = 10MBit

Please refer to section 3.1, port 1:LED1-2, port 2: LED2-2, port 3: LED3-2, port 4: LED4-2

4.2.2 EXTERNAL SWITCH VERSION (SPIDERLAN-1E, SPIDERLAN-2E)

4.2.2.1 LED5 - TRANSMIT ACTIVITY

This LED indicate transmit activity of the network controller. (data transmission to a cable connected external switch submodule (SPIMS4)). For the location of the LED please refer to section 3.1.1.1.

On = Receive Activity
Off = No Activity

4.2.2.2 LED6 - RECEIVE ACTIVITY

This LED indicate receive activity of the network controller. (data reception from a cable connected external switch submodule (SPIMS4)) For the location of the LED please refer to section 3.1.1.1.

On = Transmit Activity
Off = No Activity

4.3 5-PORT LAYER 2 SWITCH SUBSYSTEM

Each of the SPIDERLAN NIC channels can be equipped with complete 5 port switch subsystem. 1 Port is connected to onboard NIC and 4 ports are available on RJ45 connectors.

4.3.1 ADVANTAGES OF SWITCHED NETWORKING

Unlike hubs, switches operate at the data link layer (layer 2) of the OSI reference model. Each packet which is received, will be examined and processed, rather then simply repeated. The MAC addresses of the nodes residing on each network segment are mapped and only the necessary traffic is allowed to pass through the switch. Additionally, bad or misaligned packets are prevented from spreading by not forwarding them. Packet filtering and regeneration enables to split the network into separate collision domains. In switched networks, each segment is an independent collision domain. This allows greater distances, more nodes and lowers the overall collision rates. Another advantage is that the ports can work with different data rates (10 or 100Mbit) or with half /full duplex.

4.3.2 ADDRESS LOOK UP

The switch controller provides a look up engine with a internal look up table, that stores MAC addresses and their associated information. It contains 1K full CAM with 48-bit address plus switching information. It is guaranteed to learn 1K addresses and distinguishes itself from hash-based look up tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

4.3.2.1 LEARNING

The look up engine will update its table with a new entry if the following conditions are met:

(1) The received packet's source MAC address (SA) does not exist in the look up table.

(2) The received packet is good; the packet has no receiving errors, and is of legal length.

The look up engine will insert the qualified source MAC address (SA) into the table, along with the port number, time stamp. If the table is full, the last entry of the table will be deleted first to make room for the new entry.

4.3.2.2 MIGRATION

The look up engine also monitors whether a station is moved. If it happens, it will update the table accordingly. Migration happens when the following conditions are met:

(1) The received packet's source MAC address (SA) is in the table but the associated source port information is different.

(2) The received packet is good; the packet has no receiving errors, and is of legal length.

The look up engine will update the existing record in the table with the new source port information.

4.3.2.3 AGING

Aging is the amount of time the switch waits until it removes a source MAC address (SA) from the look up table due the fact that the source address has not initiated a transmission within the aging time,
The look up engine will update the time stamp information of a record whenever the corresponding source MAC address (SA) appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look up engine will then remove the record from the table. The look up engine constantly performs the aging process and will continuously remove aging records. The aging period is set to 300 seconds.

4.3.2.4 FORWARDING

The packets will be forwarded as follows:

(1) If the destination MAC address (DA) look up results is a "match", the destination port information will be used to determine where the packet goes.

(2) If the destination MAC address (DA) look up result is a "miss", the packet will be forwarded to all other ports except the port that received the packet.

(3) All the multicast and broadcast packets will be forwarded to all other ports except the source port.

The following packets will not be forwarded:

(1) Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.

(2) 802.3x pause frames. These packets will be intercepted and do the appropriate actions.

(3) "Local" packets. Based on destination address (DA) look up. If thedestination port from the look up table matches the port where the packet wasfrom, the packet is defined as "local".

4.3.3 SWITCHING ENGINE

A very high performance switching engine moves the data to and from the MAC's and packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency. It has in internal buffer for frames that is 32Kx32 (128KB). This resource is shared between the five ports. Each buffer is sized at 128Bytes and therefore there are a total of 1024 buffers available. A per port maximum is set to 205 buffers per port.

4.3.4 MAC OPERATION

The switch controller strictly abides by IEEE 802.3 standard to maximize compatibility.

4.3.4.1 INTER PACKET GAP (IPG).

If a frame is successfully transmitted, the 96 bit time IPG is measured between the two consecutive TXEN. If the current packet is experiencing collision, the 96 bit time IPG is measured from CRS and the next TXEN.

4.3.4.2 BACKOFF ALGORITHM

The switch controller implements the IEEE Std 802.3 binary exponential back-off algorithm and "aggressive mode" back off.

4.3.4.3 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet will be dropped.

4.3.4.4 ILLEAGAL FRAMES

Illegal size frames will be discarded, as defined by the IEEE Std 802.3u, including short frames (less than 64 bytes), long frames (greater than 1522 bytes), and FCS error frames. VLAN tagged frames are treated as regular frames and any VLAN related functions will not performed. The switch should be treated as a single VLAN domain. VLAN frames will be dropped, if the size is larger than 1522 bytes and non-VLAN frames, if the size is larger than 1518 bytes.

4.3.4.5 FLOW CONTROL

Standard 802.3x flow control frames on both, transmit and receive sides, are supported. On the receive side, if a pause control frame is received, the next normal frame will not be transmitted, until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the switch controller will be transmitted. On the transmit side, the switch controller has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues. A port, which just received a packet, will be flow controlled, if the destination port resource is being used up. A flow control frame (XOFF), will be issued, containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the other flow control frame (XON) with zero pause time will be send out, to turn off the flow control (turn on transmission to the port). A hysterisis feature is provided to prevent flow control mechanism from being activated and deactivated too many times. All ports will flow controlled, if the receive queue becomes full.

4.3.4.6 HALF DUPLEX BACK PRESSURE

Half duplex back pressure (Note: not in 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full duplex mode. If back pressure is required, the switch controller will send preambles to defer other stations transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, carrier sense type back pressure will be active again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets. This scheme is better than collision based back pressure. The switch controller also supports collision based flow control. If the destination port is congested, the incoming packets will be collided to achieve back pressure.

4.3.5 BROADCAST STORM PROTECTION

The switch controller has an intelligent way to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports, except the source port, and thus will use too many switch resources (bandwidth and available space in transmit queues). Broadcast or multicast packets will be discarded, if the number of those packets exceeds 25% of the network line rate in preset period of time. If the preset period expires, it will then resume receiving broadcast or multicast packets until the threshold is reached.

4.3.6 AUTO NEGOTIATION

All ports conforms to the auto negotiation protocol as described by the 802.3 committee. Auto negotiation allows UTP (Unshielded Twisted Pair) link partners to select the best common mode of operation. In auto negotiation the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner is forced to bypass auto negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol. The flow for the link set up is depicted below.

5. SOFTWARE

5.1 DEVICE DRIVERS

Drivers for different operating systems are available.

5.1.1 LINKS TO THE LATEST DRIVERS

The latest driver versions are also available on the internet.

- AMD Connectivity Solutions, Networking
  PCNet Family device drivers,
  http://www.amd.com

Note:
Links may have been changed in the meantime.
The latest links can also be found on the MPL homepage http://www.mpl.ch/

6. SUPPORT INFORMATION

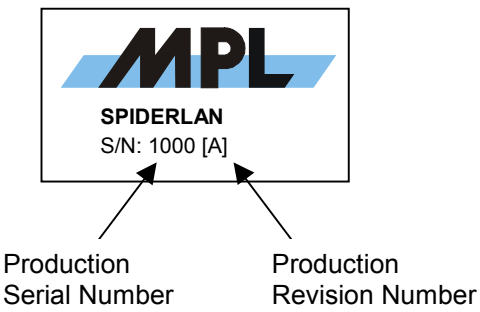
6.1 MPL AG

In case of questions contact MPL AG or your local distributor.

MPL AG homepage: www.mpl.ch
Email address: support@mpl.ch

6.2 PRODUCTION SERIAL AND REVISION NUMBER

To get the actual production revision number of your device, please see the label on the bottom of the SPIDERLAN :
housing.



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